CLAIMS

1. A method for generating a Cyclic Redundancy Check (CRC) in a system comprising the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word.

2. The method as recited in Claim 1, wherein the step of programming comprises:

programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on the pre-selected polynomial key word;

the first set of selection inputs is associated with:

selecting corresponding input from each of the logic gates; and

a shift logic that is associated with the plurality of registers.

3. The method as recited in Claim 1, wherein the step of programming comprises:

programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each of the logic gates;

the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial key word.

4. The method as recited in Claim 1, further comprising:

using a first set of multiplexers in conjunction with a first set of selection inputs for selecting at least one input for shifting data to a next shift register of the plurality of registers, wherein the at least one input is a member of a set of inputs that

includes an output from an adjacent logic gate and a straight shift input from an adjacent register of the plurality of registers.

5. The method as recited in Claim 1, further comprising:
using a second set of multiplexers in conjunction with a second set of selection inputs for selecting at least one input to a corresponding logic gate, wherein the at least one input is a member of a set of inputs that includes a primary input and a feedback input.

6. The method as recited in Claim 1, further comprising:
using a second set of multiplexers in conjunction with a second set of selection inputs for selecting a final output from among output from the plurality of registers.

7. The method as recited in Claim 1, wherein the plurality of registers are shift registers.

8. A method for generating a Cyclic Redundancy Check (CRC) generator in a system comprising the steps of:
creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and
programming a first set of selection inputs, wherein:
the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;
the first set of selection inputs is associated with:
selecting corresponding input from each of the one or more logic gates; and
a shift logic that is associated with the plurality of registers; and
programming a second set of selection inputs, wherein:
the second set of selection inputs is associated with selecting corresponding input to each logic gate;
the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.

9. The method as recited in Claim 8, further comprising:
using a first set of multiplexers in conjunction with the first set of selection inputs for selecting at least one input for shifting to a next register of the plurality of registers, wherein the at least one input is a member of a set of inputs that includes an output from an adjacent logic gate and a straight shift from an adjacent register of the plurality of registers.

10. The method as recited in Claim 8, further comprising:
using a second set of multiplexers in conjunction with the second set of selection inputs for selecting at least one input to a corresponding logic gate, wherein the at least one input is a member of a set of inputs that includes a primary input and a feedback input.

11. The method as recited in Claim 8, further comprising:
using a second set of multiplexers in conjunction with the second set of selection inputs for selecting the final output from among output from the plurality of registers.

12. The method as recited in Claim 8, wherein the plurality of registers are shift registers.

13. A computer-readable medium carrying one or more sequences of instructions for generating a Cyclic Redundancy Check (CRC) generator in a system, which instructions, when executed by one or more processors, cause the one or more processors to carry out the steps of:
creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and
programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word.

14. A computer-readable medium carrying one or more sequences of instructions for generating a Cyclic Redundancy Check (CRC) generator in a system, which instructions, when executed by one or more processors, cause the one or more processors to carry out the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;

the first set of selection inputs is associated with:

selecting corresponding input from each of the one or more logic gates; and

a shift logic that is associated with the plurality of registers; and

programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each logic gate;

the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.

15. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

means for creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

means for programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word.

16. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

means for creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

means for programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;

the first set of selection inputs is associated with:

selecting corresponding input from each of the one or more logic gates; and

a shift logic that is associated with the plurality of registers; and

means for programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each logic gate;

the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

means for the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.

17. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

a processor;

one or more stored sequences of instructions which, when executed by the processor,

cause the processor to carry out the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word.

18. An apparatus for creating a Cyclic Redundancy Check (CRC) generator in a system, comprising:

a processor;

one or more stored sequences of instructions which, when executed by the processor, cause the processor to carry out the steps of:

creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and

programming a first set of selection inputs, wherein:

the step of programming the first set of selection inputs is based on a pre-selected polynomial that is associated with the CRC generator;

the first set of selection inputs is associated with:

selecting corresponding input from each of the one or more logic gates; and

a shift logic that is associated with the plurality of registers; and

programming a second set of selection inputs, wherein:

the second set of selection inputs is associated with selecting corresponding input to each logic gate;

the second set of selection inputs is associated with selecting a final output from among output from the plurality of registers; and

the step of programming the second set of selection inputs is based on the pre-selected polynomial that is associated with the CRC generator.